Ph.D. Research Project: Developing Non-Intrusive Hybrid Fault Tolerance Techniques to Detect Errors in Multiple Processors Systems

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Introduction:

The use of fault-tolerance structures in multiple processors systems due to the fact that it is almost impossible to manufacture integrated circuits without any defect in nanometer technologies [1]. As a result, the use of fault tolerant methods is crucial to allow that circuits with some amount of defects still reach the market, increasing yield and the lifetime of a chip. A classical example comes from DRAM circuits, where defects are compensated by the use of spare rows and columns.

With the technology introduced in the past decade, the number of expected defects in high-density circuits is increasing, and fault-tolerant techniques able to detect and correct multiple faults are very expensive, in terms of area, power and performance. Aiming at reducing the overhead cost, fault tolerance features should be turn on only in the exact location of defects. In this way, fault tolerance structures would not penalize the circuit in power and/or performance in case a fault is not present.

Defects can have permanent effect, such as stuck-at, shortcut or open signals, or still show intermittent effects, like crosstalk between interconnection lines. For the above mentioned classes of defects, detection and diagnoses can be developed during manufacturing test, and off-line tests also can run during the life time of the circuit [2, 3, 4]. So, with the information of fault locations, a mechanism to deactivate a defective component and turn on a fault tolerance feature can be used. For example, in a multiple processor system, once a defect or failure has been detected in a microprocessor, the software application can be mapped on the remaining hardware components of a multiprocessor circuit [5]. Unfortunately, this simple deactivation approach cannot deal with faulty router or faulty link in the NoC, unless the NoC is modified to be able to adapt itself in the presence of faults.

In this way, we propose methods to detect faults in multiple processors systems.

Motivation:

Fault tolerance techniques for microprocessors can be based on software or hardware redundancy.

The first one is based on adding instruction redundancy and comparison to detect or correct faults. They are able to detect faults that affect the data and control flow. Software-based techniques are non-intrusive because no modifications in the hardware of the microprocessor are required. Consequently, they provide high flexibility, low development time and cost. In addition, new generations of microprocessors that do not have RadHard versions can be used. As a result, applications can use commercial of the shelve (COTS) microprocessors with RadHard software. However, software-based techniques cannot achieve full system protection due to control flow errors. This limitation is due to the inability of the software in protecting all the possible control flow effects that can occur in the microprocessor.

Hardware-based techniques usually change the original microprocessor architecture by adding logic redundancy, error detection and correction codes or majority voters. Another option is to add monitoring devices to the system in a non-intrusive way. Such techniques exploit special purpose hardware modules, called watchdog processors. Watchdogs usually can have access to the data and code memory connections. Since they only have access to the memory, watchdogs do not detect faults that are latent inside the microprocessor, as well faults in the register bank.

This research proposal targets to combines hardware-based and software-based techniques to develop hybrid fault tolerance techniques. This works aims at minimizing the performance loss caused by

software-based techniques and using hardware-based techniques to order to protect the multiple processor system against errors.

Research goals:

Realizing the importance and novelty of the issue, a research work is proposed focusing on hardware-based and software-based techniques to detect errors in multiple processor systems. The research tasks to be performed in the scope of this Ph.D. internship are:

1. **Hardware-based Techniques:** Fault tolerant techniques based on hardware usually rely on a hardware replication or additional modules. This task focuses on the research of non-intrusive hardware-based techniques implementations combining watchdog and decoder characteristics. The first will be used in order to detect incorrect jumps to unused memory addresses and control-flow loops, while the decoder characteristics will allow the module to spoof the data and address buses and the read/write signal between the microprocessor and the memory in order to execute instructions sent by the software-based transformation rules and increase the system's performance, by computing the program's flow analysis.
2. **Software-based Techniques:** Software-based instruction replication is the key to protect the system against faults. These fault tolerant techniques are described as a set of transformation rules which analyzes the program's flow and controls the hardware-based implemented modules. This task targets researching and combining software-based techniques for protecting the system against faults affecting the data path, the control path and also controlling the hardware-based module.
3. **Condor:** As part of the project Heterogeneous Converged Metro/Access Infrastructure (CONDOR) a heterogeneous multiple processor system-on-chip will be developed in order to process optical signals transmitted with OFDM. To achieve the required data rate of several gigabits, the system with process multiple data streams in parallel by different cores. Such system requires a high reliability and the detection and correction of errors during the communication between different cores. This application will be hardened as a case-study scenario.
4. **Accordance:** The EU project A Copper-Converged Optical OFDMA radio-based access network with high capacity and flexibility (ACCORDANCE) focus on developing a high performance OFDMA system with high data rates over optical networks. The total data rate of the system is over 50 Gbit/s and therefore requires a complex and highly parallel digital signal processing system. The required system must be built upon a heterogeneous network controlled by a variety of microprocessors and monitors. This system is distributed across multiple FPGAs, which have high requirements concerning the reliability of the interconnection between structures. This EU project will also be used as a case-study scenario for the techniques developed in the PhD research.

References:

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